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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/680,665	10/06/2003	George Matamis	SNDK.294US0	5425

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EXAMINER	
DOTY, HEATHER ANNE	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 06/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/680,665	MATAMIS ET AL.	
	Examiner	Art Unit	
	Heather A. Doty	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *22-26* is/are allowed.

6)☒ Claim(s) *1,3-6,8 and 10-19* is/are rejected.

7)☒ Claim(s) *2,7,9,20 and 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/03, 12/5/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *IDS 7/27/04*.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-6, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aritome et al. (U.S. 5,528,547) in view of Ogura et al. (U.S. 5,650,345).

With respect to claim 1, Aritome et al. teaches a NAND cell type EEPROM formed from a substrate, the device comprising strings of transistors of a NAND architecture comprising a first select gate (QS1 in Figs. 1 and 2), a plurality of floating gates (16 in Fig. 2), and a second select gate (QS2 in Figs. 1 and 2), each floating gate having at least two sides perpendicular to the axes of the strings Fig. 2). Aritome et al. does not teach a conductive isolating member adjacent to each of the at least two perpendicular sides of the floating gate and located between adjacent transistors in the strings of transistors, each isolating member shielding a selected floating gate from a charge stored in an adjacent component.

Ogura et al. teaches a conductive member adjacent to each of the at least two perpendicular sides of a floating gate (**82** in Fig. 8).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Aritome et al. by adding a conductive member adjacent to each of the at least two perpendicular sides of the floating gate and

located between adjacent transistors in the strings of transistors, as taught by Ogura et al., which would isolate the floating gate from adjacent floating gates in the string.

The motivation for doing so at the time of the invention would have been to increase the capacitive coupling to the floating gate, which avoids problems of increased erasing and programming voltages, as expressly taught by Ogura et al. (column 5, lines 15-23).

With respect to claim 3, Ogura et al. further teaches that the isolating members have two principal faces, the faces substantially parallel to the at least two sides of each floating gate and substantially perpendicular to the axes of the strings (Fig 8).

With respect to claim 4, Ogura et al. further teaches that the isolating members extend a distance between the substrate and an upper level of the floating gates (floating gate **50** in Fig. 5, conductive sidewall **82** in Fig. 8).

With respect to claim 5, Ogura et al. further teaches that the floating gates have an upper level and lower level, the isolating members extending from the substrate a distance between the lower and upper level (Fig. 8 shows that the lower level of the floating gate is at the substrate, and the isolating member extends upward from the substrate).

With respect to claim 6, Ogura et al. further teaches that the isolating members and the wordlines comprise a conductive material, and the isolating members are electrically connected to a wordline above a floating gate that the isolating members shield (Fig. 1 shows wordline (control electrode layer 18) extending vertically between III

and III; Fig. 8 shows control gate in contact with conductive isolating sidewall spacers; column 5, lines 15-17).

With respect to claim 8, because the combined teachings of Aritome et al. and Ogura et al. include a conductive isolating member between adjacent floating gates, the result is a flash memory device, wherein the isolating members shield a floating gate of the plurality of floating gates from an electrical field of an adjacent floating gate, thereby minimizing field effect coupling between adjacent floating gates.

Claims 10-16, 18, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (U.S. 6,689,658) in view of Fukumoto et al. (U.S. 2002/0096704).

With respect to claim 10, Wu teaches a non-volatile memory device comprising floating gates that store a charge (**302a** in Fig. 4G(a)); bitlines that select amongst the floating gates, each bitline having a bitline axis (Fig. 2A); wordlines that select amongst the floating gates (Fig. 2A); and sidewall elements positioned along the bitline axes, the sidewall elements located at sides of the floating gates between adjacent floating gates (**310a** in Fig. 4G(a)). Wu does not teach that the sidewall elements shield the floating gates.

Fukumoto et al. teaches conductive sidewall elements that shield floating gates (25 in Fig. 1A).

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the memory device taught by Wu by fabricating the sidewall elements of a conductive material, as taught by Fukumoto et al., which would result in the sidewall elements shielding the floating gates.

The motivation for doing so at the time of the invention would have been to shield an insulating film between a floating gate and a control gate from electric fields, as expressly taught by Fukumoto et al. (paragraphs 0028 and 0030).

With respect to claim 11, the conductive sidewall elements taught by Wu and Fukumoto et al. together will shield the floating gates from an electrical field having a component in the direction of the bitline axis.

With respect to claims 12, 13, and 14, the conductive sidewall elements taught by Wu and Fukumoto et al. together extend from the substrate to the floating gates, until or beyond the level of the lowermost surface of the floating gates, and until or beyond the level of the uppermost surface of the floating gates. (Wu, Fig. 4G(a)).

With respect to claims 15 and 16, Wu and Fukumoto et al. together teach the memory device of claim 10 wherein the sidewall elements comprise a conductive material, and wherein the sidewall elements are electrically coupled to a wordline located between adjacent pairs of sidewall elements (Wu, Fig. 4G(a) shows conductive wordlines **307a** in contact with sidewall spacers **310a** that are conductive, as taught by Wu and Fukumoto et al. together), so that the surface area of the wordline and the electrical coupling between the wordline and the floating gates are effectively increased.

With respect to claim 18, Wu teaches a method of forming NAND flash memory comprising forming floating gates (**302a** in Fig. 4G(a)); forming control gates above the floating gates (**307a** in Fig. 4G(a)); forming bitlines, the bitlines used together with the control gates to read and write from a floating gate, the direction of the bitlines substantially perpendicular to the direction of the control gates (Fig. 2), the floating

gates having bitline sides in the bitline direction and control gate sides in the control gate direction (Fig. 4G(a)); and forming members on the bitline sides of the floating gates (**310a** in Fig. 4G(a)). Wu does not teach that the members shield the floating gates from electrical fields having a component in the bitline direction.

Fukumoto et al. teaches a method of forming floating gates with conductive sidewall spacers that shield the floating gates from electrical fields having a component in the bitline direction.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Wu by fabricating the isolating members of a conductive material, as taught by Fukumoto et al.

The motivation for doing so at the time of the invention would have been to shield an insulating film between a floating gate and a control gate from electric fields, as expressly taught by Fukumoto et al. (paragraphs 0028 and 0030).

With respect to claim 19, Wu teaches a flash memory device comprising floating gates (**302a** in Fig. 4G(a)) for storing data located above a substrate (**300** in Fig. 4G(a)); means for isolating adjacent floating gates in the wordline direction (STI lines in Fig. 2A); means for isolating adjacent floating gates in the bitline direction (sidewall spacers **310a** in Fig. 4G(a)); and means for reading the data stored in the floating gates (wordlines 307a in Fig. 4G(a)), the means for reading the data located above the floating gates and interconnecting strings of floating gates (Figs. 2, 4G(a)). Wu does not teach that the means for isolating adjacent floating gates in the bitline direction is electrically connected to the means for reading the data.

Fukumoto et al. teaches conductive sidewall spacers on floating gates in a flash memory device.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to modify the teachings of Wu by fabricating the isolating sidewall spacers of a conductive material, as taught by Fukumoto et al., which would result in an electrical connection between the means for isolating adjacent floating gates in the bitline direction (conductive sidewall spacers) and the means for reading the data (conductive wordlines, see Fig. 4G(a)).

The motivation for doing so at the time of the invention would have been to shield an insulating film between a floating gate and a control gate from electric fields, as expressly taught by Fukumoto et al. (paragraphs 0028 and 0030).

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wu (U.S. 6,689,658) in view of Fukumoto et al. (U.S. 2002/0096704) as applied to claim 10 above, and further in view of Lee et al. (U.S. 2002/0028541).

With respect to claim 17, Wu and Fukumoto et al. together teach the memory device of claim 10 (note 35 U.S.C. 103(a) rejection above). Wu further teaches that the device is a NAND flash memory (column 1, lines 7-10; column 12, lines 6-10). They do not teach that the wordline extends between adjacent floating gates so as to shield a selected floating gate from an electrical field of adjacent floating gates.

Lee et al. teaches forming a wordline that extends between adjacent floating gates.

Therefore, at the time of the invention, it would have been obvious to one of ordinary skill in the art to fabricate the memory device as taught by claim 10 and by Wu and Fukumoto et al. together, and add a wordline that extends between adjacent floating gates, as taught by Lee et al. The resulting invention would shield a selected floating gate from an electrical field of adjacent floating gates, since the conductive wordlines would extend between the floating gates.

The motivation for doing so at the time of the invention would have been to increase the area between the floating gate and the wordline, which increases the capacitive coupling between the floating gate and the wordline, as expressly taught by Lee et al. (paragraph 0252).

Allowable Subject Matter

Claims 2, 7, 9, 20, and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 22-26 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Prior art does not teach or suggest, in combination with the other claimed limitations, wordlines that extend between floating gates into shallow trench isolation areas, thereby isolating adjacent floating gates, or T-shaped floating gates flanked by wordlines that are electrically coupled to isolating members between adjacent floating gates. Lee et al. (U.S. 2002/0028541) teaches T-shaped floating gates flanked by wordlines (Fig. 51), but the wordlines are not electrically coupled to the sidewall spacers between adjacent floating gates (a layer of dielectric separates the wordlines from the sidewall spacer, which itself is insulating). Furthermore, Lee et al. teaches a wordline that extends between floating gates, but into the source/drain regions, not into shallow trench isolation regions.

Prior art also does not teach or suggest shielding floating gates from adjacent floating gates that are diagonally or horizontally adjacent to the selected floating gate.

Finally, prior art does not teach or suggest forming a second set of parallel trenches in an oxide layer deposited within a first set of trenches and then forming wordlines that extend between adjacent floating gates into the second set of trenches.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Heather A. Doty, whose telephone number is 571-272-8429. The examiner can normally be reached on M-F, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

had

Craig A. Thompson

CRAIG A. THOMPSON
PRIMARY EXAMINER